2025-12-17

BASIC CMOS VLSI DESIGN

Department of Electronics and Communication Engineering

SRM UNIVERSITY A.P

Registration Number: _____

Name: _____

Branch & Section: _____

SRM UNIVERSITY AP
Andhra Pradesh

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End Term Examination, Dec 2025

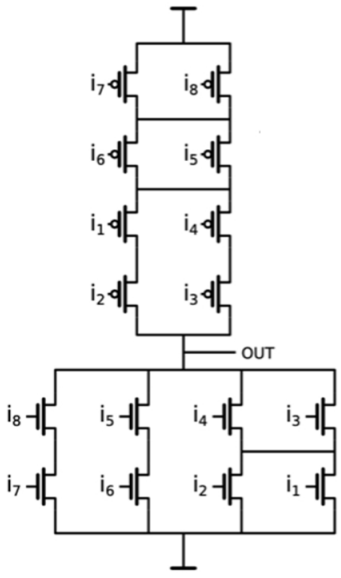
[Question Paper ID: **010701]**

Subject Title	: BASIC CMOS VLSI DESIGN	**Subject Code**	: ECE 301
Batch	: 2023	**Max Marks**	: 50
Degree	: B.Tech.	**Duration**	: 2 hours
Branch	: ECE	**QP Set**	: 1

Section A (5 × 4 = 20 Marks)

Answer **any 5** Questions

		Marks	CO	BL
1.	Explain why the size of PMOS is two times higher than the size of NMOS in the CMOS Inverter.	**4**	**1,3**	**2**
2.	Construct t**wo input AND and NAND gates** using the following switch logic, **(A)** Pass Transistor Logic, **(B)** Transmission Gate Logic.	**4**	**1,3**	**3**
3.	Derive and compare the scaling factors of **Constant field** and **Constant voltage scaling** in terms of **(a)** Oxide Capacitance, **(b)** Drain Current, **(c)** Power Dissipation, and **(d)** On Resistance (R_{on}).	**4**	**1,2,3**	**4**
4.	Define the **Logical Effort** of a CMOS gate, and calculate the logical effort of a **two-input CMOS NAND** gate.	**4**	**1,2,3**	**2**
5.	List the important timing metrics to be followed for the successful design of **CMOS sequential circuits**.	**4**	**1,2,3,4**	
6.	For the CMOS circuit shown below, find **(a)** Boolean expression, and **(b)** Size each transistor with respect to the standard CMOS inverter.	**4**	**1,2,3**	**1**



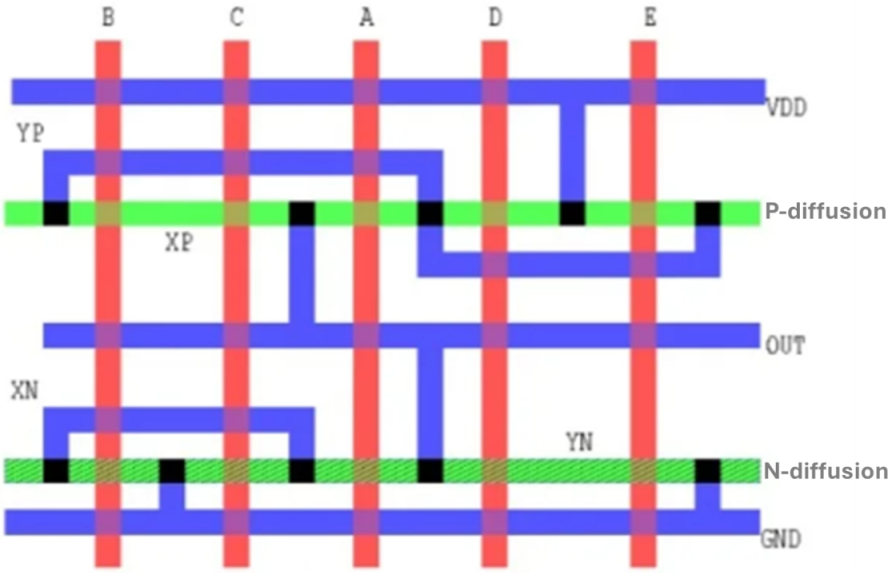
7.	Given two NMOS transistors (**MOS1** and **MOS2**) with W/L ratios of 2 and 10, respectively. Identify which transistor will have **high On resistance** (R_{on}) and why?. (Note: Except W/L ratio, all remaining parameters are same for both transistors).	**4**	**1,2,3,4**	

		Marks	CO	BL
8.	Draw the capacitive model of MOSFET and list all the capacitive components that contribute to each capacitance in the model.	4	1,2,3	4

Section B (5 × 6 = 30 Marks)

Answer **any 5** Questions

		Marks	CO	BL
9.	Given, μ_n = 1000 cm^2/V sec, Cox = 5 fF/μm^2, W = 20 µm, L= 0.2 µm, V_{TH} = 0.5 V, V_{GS} = 1 V and V_{DS} = 0.8 V, solve the following **(a)** Identify the region of operation, **(b)** Transistor gain factor (β), **(c)** Drain Current (I_D), **(d)** Gate Capacitance (Cg), **(e)** Transconductance (g_m), **(f)** Figure of Merit (ωo).	6	1,2,3	3
10.	Analyze the layout circuit shown below and draw **(a)** Stick Diagram and **(b)** Schematic diagram, and **(c)** Boolean function.	6	1,2,3	4



11.	For the Boolean function shown below, **(a)** draw CMOS Schematic diagram, **(b)** Size each transistor to match the currents of PMOS-PUN and NMOS-PDN. **F = (A+BC)'(DE)'(F'+G').**	6	1,2,3	4
12.	Design a **Half Adder** using CMOS logic with a minimum number of NMOS & PMOS transistors. Also, for better design, analyze the logic circuit and find the **optimum size of each transistor**.	6	1,2,3,4	
13.	Draw and explain the working operation of a **single-bit SRAM** cell.	6	1,2,3,4	
14.	**(a)** Calculate the normalized propagation delay (t_p/t_{p0}) of the **(i) Unbuffered** and **(ii) Dual stage inverter design**, when **γ = 1**, and **F = 100**. **(2 Marks)** **(b)** Identify the **optimum number of stages** of the inverter chain, with respect to the propagation delay for **γ = 1 and F = 100**. **(4 Marks)**	6	1,2,3,4	
15.	**(a)** Construct **4:1 MUX** using **(i)** NMOS Pass Transistor Logic (PTL), **(ii)** Transmission Gate Logic (TGL) with a minimum number of transistors. **(5 Marks)** **(b)** In comparison of PTL with TGL, write the major drawback of PTL over TGL. **(1 Mark)**	6	1,2,3,4	

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