DIGITAL DESIGN WITH HDL

Department of Electronics and Communication Engineering

SRM UNIVERSITY A.P

Registration Number: _____

Name: _____

Branch & Section: _____

SRM UNIVERSITY AP
Andhra Pradesh

SRM UNIVERSITY – AP, ANDHRA PRADESH

End Term Examination, Dec 2025

[Question Paper ID: **010690]**

Subject Title	: DIGITAL DESIGN WITH HDL	**Subject Code**	: ECE 201
Batch	: 2024	**Max Marks**	: 50
Degree	: B.Tech.	**Duration**	: 2 hours
Branch	: ECE	**QP Set**	: 1

A (5 × 10 = 50 Marks)

Answer **any 5** Questions

		Marks	CO	BL
1.	Consider a digital lock that opens only when a correct sequence of digits is entered. Determine whether it represents a combinational or sequential circuit and explain your reasoning. Explain D flip flop.	**10**	**3,4**	**2**
2.	Design and verify the conversion of a JK flip-flop into a D flip-flop using logic equations and excitation mapping.	**10**	**3,4**	**5**
3.	Design and verify the Verilog code for a Full Subtractor circuit. Include necessary comments, logic explanation, and testbench structure.	**10**	**2,3,4**	**5**
4.	Design a 1×8 Demultiplexer using 1×2 Demultiplexers. Illustrate the hierarchical design, draw the logic diagram, and explain the signal routing.	**10**	**3,4**	**3**
5.	Design and verify a Full Subtractor using Multiplexers. Include the truth table, Boolean reduction steps, and block-level schematic.	**10**	**2,3**	**6**
6.	Design and verify a Full Subtractor using a Decoder. Include truth table, Boolean simplification, and block-level schematic.	**10**	**3,4**	**6**

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